長庚大學 112 學年度第二學期 資訊工程學系博士班資格考 計算機架構 考題

1. RISC (Reduced Instruction Set Computer) is the trend of current processor architecture.
   (a) List two characteristics of the RISC instruction set architecture.
   (b) Explain why these characteristics can improve the performance of a processor.

   (10/10 points)

2. Cache design will affect the data access time for a processor.
   (a) List two possible data placement policies for a cache and explain how they work.
   (b) Compare the differences in performance between the policies you answer in (a).

   (10/10 points)

3. There are two instruction scheduling approaches to enhance a processor's performance by exploiting more instruction level parallelism: static instruction scheduling and dynamic instruction scheduling.
   (a) For each of them give an example to show how did they work.
   (b) For a graphic application (e.g., matrix operations), which one is better? Give your reasons.

   (10/10 points)

4. A compiler can increase the data locality by translating data access sequence to speedup data access time from cache.
   (a) Use an example to show how can a compiler increase the "temporal locality" for data access in a program.
   (b) Use an example to show how can a compiler increase the "spatial locality" for data access in a program.

   (10/10 points)

5. The virtual memory design can enhance the memory management.
   (a) Explain how to reduce the data access time in a virtual memory system.
   (b) Can we implement the cache design in a virtual memory system? If yes, how? If no, why?

   (10/10 points)