電機工程學系博士班(資工領域)102 學年度第 2 學期資格考試試題

考試科目：計算機架構

(2014 Qualify Exam, Computer Architecture)

1. List and explain any two approaches which can improve the miss rates of a cache system. Also, you have to discuss what the drawbacks they may have.

   (20 points; each 10 points)

2. There are two kinds of approaches which can exploit the instruction level parallelism: dynamic scheduling algorithms (e.g., Tomasulo's algorithm) and static scheduling algorithms (e.g., Loop unrolling). Answer the following questions.

   (a) In what cases the dynamic instruction scheduling algorithms can exploit more parallelism in a program than the static instruction scheduling algorithms? Use an example to explain your answer.

   (b) In what cases the static instruction scheduling algorithms may perform better than the dynamic instruction algorithms? Use an example to explain your answer.

   (20 points; each 10 points)

3. In a computing system supporting the "virtual memory" mechanism, address translation between the virtual address and the physical address would be a major performance bottleneck for each cache access. Answer the following questions.
   (a) Explain how to speedup the address tranlation in a virtual memory system.
   (b) If such a system allows multiple processes to be activated at the same time, what problem will we meet possibly? How to solve it?

   (20 points; each 10 points)

4. There are two processors which have the same instruction set architecture. All instructions can be partitioned into four classes: Arithmetic, Load, Store, and Branch. The clock rate and CPI (cycles per instruction) of each implementation are given in the following table.

	Clock rate	Arithmetic CPI	Load CPI	Store CPI	Branch CPI
Processor 1	2 GHz	3	2	2	1
Processor 2	3 GHz	4	3	3	2

   (a) Assume that a program totally has 10^6 instructions. This program contains 30% Arithmetic, 30% Load, 20% Store, and 20% Branch instructions. Which processor is faster and by how much for this program?
   (b) Continue with (a). If the number of the Arithmetic instructions can be reduced

by a half, which processor is faster and by how much?

(c) Now we have another program which can be divided into 40% Arithmetic, 20% Load, 15% Store, and 25% Branch instructions. If we modify processor 2 by improving its Arithmetic logic 4 times faster, how much overall speedup we can obtain after the modification, compared with original processor 2?

(30 points; each 10 points)

5. For modern multicore processors, the thread-level parallelism exploitation is more important than the instruction-level parallelism exploitation. Why?

(10 points)