Qualifying Examination: Computer Architecture (September 2014)

1. Explain the difference between superscalar and VLIW (Very Long Instruction Word) processors. Give application scenarios (practical industry applications) for the two kinds of processors. (20 pts)
2. Give example program fragments to explain each of the following hazards. (20 pts)
   (a) RAW (read after write) data hazard
   (b) WAW (write after write) data hazard
   (c) WAR (write after read) data hazard
   (d) Control hazard
3. Give an example, with a program fragment and the pipeline behavior, to explain why branch prediction may improve the performance of a pipelined processor. (20 pts)
4. Explain why a multi-core processor needs a cache coherence protocol. Give an example of a cache coherence protocol and show how it works. (20 pts)
5. Give an example, with a program fragment and a cache organization, to explain how compiler optimization may help to improve the hit rate of a cache. (20 pts)