電機工程學系博士班(資工領域)101 學年度資格考試試題

考試科目：計算機架構

1. Flynn (1966) proposed a simple model of categorizing all computers that is still useful today. We usually call this model “the taxonomy of parallel architectures” or just say “Flynn’s classification”. In this model, there are four categories which represent four kinds of parallelism relationships between the instruction and data streams. Explain each of the categories in the Flynn’s classification. (20%)

2. A typical scalar processor (e.g., MIPS processor) contains five basic pipeline stages:
   (i) Instruction fetch: fetch instruction from memory
   (ii) Decode and read operand: read registers while decoding the instruction
   (iii) Execution: execute the operation or calculate the address
   (iv) Memory access: Access an operand in data memory
   (v) Write back: Write the result into a register

   Based on this pipeline architecture, answer the following questions.

(a) It is impractical to require that all operations complete in 1 clock cycle, or even in 2. For example, the multiply or floating-point operations always need longer latency. As a result, the third stage (i.e., Execution) may be repeated as many times as needed to complete the operation. If so, implementing this 5-stage pipeline will face many challenges in hazard detection and exception handling. Why? Use examples to explain the reasons. (10%)

(b) The implementation of the “dynamic instruction scheduling” can improve the pipeline performance by exploiting more instruction-level parallelism. How to modify this 5-stage pipeline such that the processor can support the feature of the “dynamic instruction scheduling”? (10%)

(c) The implementation of the “hardware-based speculation” can avoid pipeline stalls from control hazards. How to modify this 5-stage pipeline such that the processor can support the feature of the “hardware-based speculation”? (10%)

3. The importance of the memory hierarchy has increased with advances in performance of processors. We call the gap in performance between memory and processors “the processor-memory gap”. The design of the “Cache” is one of the most important solutions to close the processor-memory gap. List any three of cache designs (no matter hardware or software) which can improve cache performance, and explain why they can improve it. (30%)

4. In a multiprocessor system, what is the cache coherence problem? (10%)
   Design an algorithm or a protocol to resolve the cache coherence problem between multiple processors. (10%)