1. Fig. 1 shows the structure of a quad-core processor with the hyper-threading technology which is originally proposed by Intel. In this structure, Core 1 and Core 2 share a common cache, while Core 3 and Core 4 share another one. Explain the following questions.
   (a) Why the designer let (Core 1, Core 2) or (Core 3, Core 4) share a common cache? If you are a designer, what problem should we notice for such a kind of shared cache structure? (10 points)
   (b) Why the designer does not let (Core 1, Core 2) and (Core 3, Core 4) share a common cache? If you are a designer, what problem should we notice for such a kind of split cache structure? (10 points)

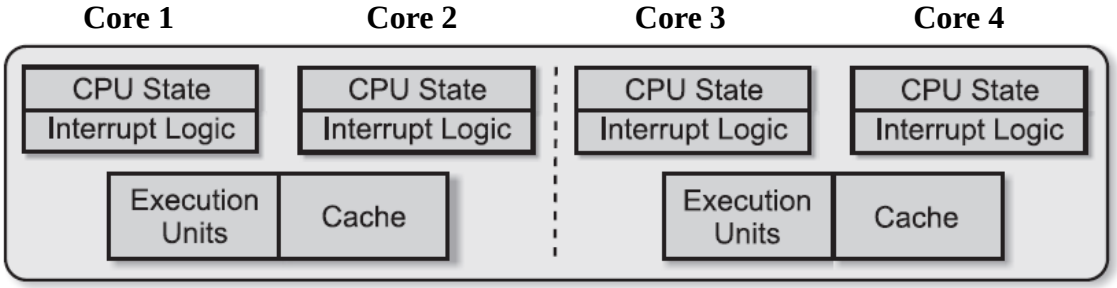

Fig. 1 A quad-core processor with the hyper-threading technology

2. There are some challenges when applying the parallel processing techniques to computer architecture (e.g., parallel processors) design. List any two of challenges and explain why they are indeed the challenges. (10 points)

3. The importance of the memory hierarchy, especially the cache design, has increased with the advances in performance of processors.
   (a) List and explain any two techniques to reduce the cache hit time. (10 points)
   (b) Compiler optimizations can reduce the cache miss rate through loop transformations. Use an example to show how to do it. (10 points)

4. Three enhancement designs with the following speedups are proposed for a processor:
   Enhancement design 1's speedup=5
   Enhancement design 2's speedup =4

Enhancement design 3's speedup =2

(a) Assume that all of three enhancement designs are implemented in the processor. If enhancement design 1 and design 2 are each usable for 20% of the time, what fraction of the time must enhancement design 3 be used to achieve an overall speedup of 2? (10 points)

(b) Assume only two of them can be implemented in the processor. For a given benchmark, the possible fraction of use is 25%, 24%, and 30% for each of enhancement designs 1, 2, and 3, respectively. Which two enhancements should we choose to maximize the overall performance? (10 points)

5. Use an example to show that the loop-unrolling algorithm can improve loop-level parallelism with loop scheduling.

(10 points)

6. Explain the differences between the dynamic scheduling approach and the static scheduling approach in exploiting the instruction level parallelism (ILP)?

(10 points)

7. The superscalar architecture and the VLIW (Very Long Instruction Word) architecture dominate most of modern processor designs. Explain their differences.

(10 points)