電機工程學系博士班(資工領域)102 學年度資格考試試題

考試科目：計算機架構

1. The “Virtual Memory” and the “Virtual Machines” are two of the most important protection designs for a computer. Explain how to implement each design and what are the differences between two of them? (20%)

2. Exploiting the “parallelism” in a program could speedup the execution performance for a computer. There are two types of parallelism: instruction-level parallelism and loop-level parallelism.
   (a) Use one example to explain the differences between these two types of parallelism. (10%)
   (b) List one method (hardware or software) for each of them and explain how the methods you listed can exploit the parallelism. (10%)

3. The multi-core architecture dominates most of processor designs today. Answer the following questions.
   (a) Some multi-core processors will use the “shared memory mechanism” which creates a physical memory to be shared by different cores for data communication. If so, the cache coherence problem will be introduced if different cores access the same data on the shared memory. Use an example to explain why. (10%)
   (b) Continued with question (a), how to avoid this problem for the “shared memory” mechanism? (10 %)
   (c) Instead of using the “shared memory mechanism”, some multi-core processors may use the “distributed memory” mechanism for data communication between different cores. Does the cache coherence problem still exist? If no, why? If yes, how to avoid it? (20%)

4. While a typical scalar processor (e.g., MIPS processor) contains 5 basic pipeline stages, some advanced processors may extend to 20 pipeline stages (e.g., Intel Pentium 4). When we increase the pipeline depth (i.e., from 5-stage to 20-stage), what challenges will be introduced when we apply the dynammic scheduling algorithms (e.g., Tomasulo algorithm) for instruction-level parallelism (ILP) exploitation? (List at least four possible challenges) (20%)