長庚大學電 機 工 程 學 系 (資工領域) 博士班資格考計 算 機 架 構 考 題

1. **(20 pts)** Briefly explain the design philosophy of RISC (Reduced Instruction Set Computer) processors and compare to the opponent: CISC (Complex Instruction Set Computer) processors.

2. Briefly explain the basic concepts of virtual memory system by answering the following questions
   (a) **(6 pts)** What is virtual memory?
   (b) **(6 pts)** From the programmer's view point, what is the advantage of a computer system with virtual memory?
   (c) **(8 pts)** List the hardware support required for a virtual memory system.

3. **(10 pts)** Explain why the cache memory can speed-up the program execution performance.

4. **(20 pts)** Explain the concepts about data hazard through answering the following questions.
   (a) What is a data hazard? List all types of data hazards with examples for each hazard.
   (b) Give a program example to explain how data hazards slow-down the execution of an instruction-level parallel processor.
   (c) Explain how a compiler overcomes the data hazards to exploit instruction-level parallelism. Give an example of program transformation to explain the concepts.
   (d) Explain how a hardware mechanism overcomes the data hazards to exploit instruction-level parallelism. Draw simple hardware diagram to explain the concepts.

5. **(20 pts)** Give an example, with a program fragment and a cache organization, to explain how compiler optimization may help to improve the hit rate of a cache.

6. **(10 pts)** Give an example to explain why a multi-core processor needs cache-coherence protocol.